

# TD Release Notes

===== March 2020 (r4.6.4) =====

## Updates & fixes:

1. IP Generator:
  - a) PLL: fix a crash issue while selecting CLK1 as feedback path.
  - b) BRAM: correct the valid width list for byte enable mode.
  - c) EG\_LOGIC\_BUFIO can work properly now.
  - d) RAMFIFO: fix a bug that RE may not take effect correctly in some circumstances.
2. Device Setting:
  - a) Jtagen pin will be set to dedicate while tdi\_tms\_tck\_tdo pins are set to gpio.
  - b) Remove duplicated P24 pin from EG4S20NG88.
3. IO Constraint:
  - a) The default value of drivestrength will be update along with IOStandard settings.
  - b) Remove dual-purpose pin as output LVDS on QFN88 package.
4. Synthesis:
  - a) Opt\_mux: add multiplexer optimization in order to reduce area.
  - b) Set the default value of undriven inout pin as tribuf.
  - c) Fix an adder optimization bug if the adder is driven by itself.
  - d) Fix a crash issue while try to instantiate a RAM with long initial value.
  - e) Fix a bug in EF2/EF3 pad simulation models.
  - f) Syn\_ip\_flow: ip.v/ipr.v are a little changed when syn\_ip\_flow turn to ON option.  
Usage: TD User Guide → 5.7 syn\_ip\_flow
  - g) Deal with the INV signal from syn\_ip.v more properly.
  - h) Disable redundant "KEEP" warnings in some circumstances.
  - i) Fix a bug in 'REGMODE' setting while inferring ROM.
5. Physical:
  - a) Improve routing strategy so that the pad instance driving by dual-edge could work correctly.
  - b) Fix some IOCLK related routing issues so that output of PLL could reach IOCLK correctly now.
6. Download:
  - a) Fix a device recognition issue for eagle\_15.
  - b) Fix a SPI readback bug if only read back one byte.
  - c) Fix the IO unstable during configuration issue for EG4A.
7. Device Chain:
  - a) Add EF1 family support.
  - b) Add device selection function to support multi-cables situation.
  - c) Support start address setting for Jtag studio.
8. Timing Analysis
  - a) Correct the delay data of output pad with IOStandard = lvcmos18 & drivestrength =

- 10mA.
- b) Fix a wrong async timing path in BRAM SDP mode.
- 9. ChipWatcher:
  - a) Improve the user experience and add more sanity check in GUI.
- 10. Export Tcl file for flow: support merge svf command.
- 11. Fix a bug of displaying hierarchical info for VHDL(top) + Verilog(sub) mixture design.
- 12. Update QT and other dependencies in order to address CVE issues.